REMARKS

Claims 10, 12-15 and 26-27 are pending in the Application. Claim 10 is an independent claim and claim 12 depends therefrom. Claim 13 is an independent claim and claims 14-15 depend therefrom. Claims 26 is an independent claim and claim 27 depends therefrom. Claims 11, 16-23, 25 and 28-40 were previously canceled. Claims 1-9 and 25 are currently canceled. Claim 27 is currently amended. Applicant respectfully requests reconsideration of the application in light of the above amendments and the following remarks.

Rejections Under 35 U.S.C. §112, First Paragraph (Claims 1-9 and 24)

In points 2-5 on pages 2-3 of the Office Action, claims 1-9 and 24 were rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement. (Office Action, Points 3-4, Pages 2-3). The Applicant respectfully traverses the rejection as previously set forth in Applicant's March 5, 2010 non-final Office Action response. However, in an effort to expedite allowance of claims 10, 12-15 and 26-27 or to simplify the issues for appeal, the Applicant has canceled claims 1-9 and 24 without prejudice. As such, the Applicant respectfully submits that the rejections of claims 1-9 and 24 under 35 U.S.C. §112, first paragraph, are moot and respectfully requests that the rejections of claims 1-9 and 24 under 35 U.S.C. §112, first paragraph, be withdrawn.

Rejections Under 35 U.S.C. §103(a) – Goldberg and Lehman (Claims 10, 12-15 and 26-27)

In points 18-25 on pages 15-26 of the Office Action, independent claims 10, 13 and 26, and dependent claims 12, 14-15 and 27 were rejected under 35 U.S.C. §103(a) as being unpatentable over Goldberg (U.S. Patent No. 6,874,062) in view of Lehman (U.S. Patent No. 6,658,437). The Applicant respectfully traverses the above-mentioned rejections for at least the

following reasons.

In order for a *prima facie* case of obviousness to be established, the Manual of Patent Examining Procedure, Rev. 6, Sep. 2007 ("MPEP") states the following:

> The key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious. The Supreme Court in KSR International Co. v. Teleflex Inc., 82 USPQ2d 1385, 1396 (2007) noted that the analysis supporting a rejection under 35 U.S.C. 103 should be made explicit. The Federal Circuit has stated that "rejections on obviousness cannot be sustained with mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness."

See the MPEP at § 2142, citing *In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006), and *KSR International Co. v. Teleflex Inc.*, 82 USPQ2d at 1396 (quoting Federal Circuit statement with approval). Further, MPEP § 2143.01 states that "the mere fact that references can be combined or modified does not render the resultant combination obvious unless the results would have been predictable to one of ordinary skill in the art" (citing *KSR International Co. v. Teleflex Inc.*, 82 USPQ2d 1385, 1396 (2007)). Additionally, if a *prima facie* case of obviousness is not established, the Applicant is under no obligation to submit evidence of nonobviousness:

> The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness.

See MPEP at § 2142.

First, the Applicant respectfully submits that there is no motivation to combine Lehman with Goldberg because Goldberg explicitly criticizes and discredits the considerable waste of storage space and prohibitive sizes of multiple buffer pool implementations as taught by Lehman. The Applicant notes that a disclosure that criticizes, discredits, or otherwise discourages the solution claimed of a second disclosure, teaches away from the combination of disclosures. *In re Fulton*, 391, F.3d 1195, 1201 (Fed. Cir. 2004). Goldberg unequivocally criticizes, discredits and otherwise discourages optimizing memory allocation using multiple buffer pools as taught by

Lehman. For example, Goldberg explicitly states that the use of multiple buffer pools as taught by Lehman "results in a considerable waste of storage space." (Goldberg, Column 2, Lines 34-35). As another example, Goldberg explicitly criticizes the amount of storage space consumed by data structures such as linked lists. (Goldberg, Column 2, Lines 35-44). Instead of multiple buffer pools and linked lists, Goldberg teaches a hierarchical bitmap structure noting that such bitmaps only require a single bit "to describe whether each section of storage is allocated, a much smaller amount of memory is associated with the use of bitmaps as compared to the use of linked lists." (Goldberg, Column 3, Lines 5-9).

One skilled in the art, upon reading Goldberg, would clearly be discouraged from using multiple buffer pools and/or linked lists to optimize memory allocation as taught by Lehman. Thus, despite Lehman's efforts to make multiple buffer pool implementations require less space to store allocation information, one of ordinary skill in the art would not have found that the combined teachings of Goldberg and Lehman suggest Applicant's claim limitations because Goldberg teaches staying away from multiple buffer pool implementations altogether.

Put simply, Goldberg could not be clearer in its criticism of multiple buffer pools and linked lists. Further, the combination of the references would be inoperable together. Because the combined teaching of Goldberg and Lehman would not have been construed by one of ordinary skill in the art as suggesting the limitations of Applicant's claims, the rejections under 35 U.S.C. §103(a) cannot be maintained.

Second, the Applicant respectfully submits that the proposed combination of references fails to teach, suggest, or disclose at least, for example, "wherein **the first state of the first logic circuit comprises a number of available memory segments in the first memory block, said number of available memory segments corresponding to at least the first state of the second logic circuit and the first state of the third logic circuit**" and "wherein **the first state of the first logic circuit is separate from the first state of the second logic circuit and the first state of the third logic circuit**," as set forth in Applicant's independent claim 10, and "**the first state of**

the first logic circuit comprises a number of available memory segments in the block of memory segments, said number of available memory segments corresponding to the first state of each of the respective second logic circuits," as recited in Applicant's independent claim 26.

The Applicant appreciates the Examiner's acknowledgement that Goldberg fails to teach "wherein the first state of the first logic circuit comprises a number of available memory segments in the first memory block, said number of available memory segments corresponding to at least the first state of the second logic circuit and the first state of the third logic circuit," as recited in Applicant's independent claim 10 (Office Action, Point 19, Page 18, Lines 2-3), and "the first state of the first logic circuit comprises a number of available memory segments in the block of memory segments, said number of available memory segments corresponding to the first state of each of the respective second logic circuits," as set forth in Applicant's independent claim 26. (Office Action, Point 24, Page 24, Lines 19-21). However, the Office Action alleges that Lehman's disclosure of a bit string teaches the Applicant's claim limitations. (Office Action, Point 19, Page 18, Lines 7-18 and Point 24, Page 25, Lines 1-12). The Applicant notes that the Office Action mischaracterizes the combination of Goldberg and Lehman, and the Applicant's claims.

For example, nothing in the combination of Goldberg and Lehman suggests replacing a bit in Goldberg's bitmap 1 with Lehman's bit string. In addition to Goldberg explicitly teaching away from using Lehman's bit string array pointers as discussed above, Lehman's bit string does not refer to a number of available memory segments in a lower level bitmap or LLB. Instead, Lehman's bit string is the lowest level (i.e., corresponds directly to memory blocks, which is different than corresponding to "at least the first state of the second logic circuit and the first state of the third logic circuit" as set forth in Applicant's independent claim 10, and "corresponding to the first state of each of the respective second logic circuits," as recited in Applicant's independent claim 26). Thus, even if Lehman's bit string could be considered a first state of a first logic circuit comprising a number of available memory segments in a first memory block (which is clearly not taught by Lehman), Lehman still fails to disclose "said number of available memory segments corresponding to at least the first state of the second logic circuit and

the first state of the third logic circuit," as recited in Applicant's independent claim 10, and "said number of available memory segments corresponding to the first state of each of the respective second logic circuits," as set forth in Applicant's independent claim 26.

As such, Lehman fails to remedy the deficiencies of Goldberg in that the combination of references clearly fail to teach "wherein **the first state of the first logic circuit comprises a number of available memory segments** in the first memory block, **said number of available memory segments corresponding to at least the first state of the second logic circuit and the first state of the third logic circuit**," as recited in Applicant's independent claim 10, and "**the first state of the first logic circuit comprises a number of available memory segments in the block of memory segments, said number of available memory segments corresponding to the first state of each of the respective second logic circuits**," as set forth in Applicant's independent claim 26. Because the combination of Goldberg in view of Lehman fails to teach or suggest all the claim limitations, a rejection under 35 U.S.C. §103(a) cannot be maintained.

As an aside, the Applicant notes that although the Office Action acknowledges that Goldberg fails to teach a first logic circuit comprises a number of available memory segments, the Office Action seems to inconsistently allege that Goldberg's "figure 6 teaches each state of a higher level bitmap comprises an available number of memory portion in a lower level bitmap (fig. 6 and related text; col. 4, lines 4-56). Applicant should note, that every bit of Bitmap 1 comprises a number of available memory sections/segments in LLB; wherein the Bitmap hierarchy depicted comprises more levels such as Bitmap 2 and Bitmap 3 (Fig. 6 and related text)." (*See e.g.*, Office Action, Point 30, Page 29, Line 20 – Page 30, Line 2). The Applicant respectfully submits that the Office Action mischaracterizes Goldberg and the Applicant's claim limitations.

Specifically, referring to the Office Action-cited Figure 6 of Goldberg, for example, bit 612 is in state "0" which merely indicates that memory sections in Bitmap 2 606 are available. However, nowhere in Goldberg is there any teaching that bit 612 indicates that 6 memory sections in Bitmap 2 606 are available. As such, the first state of bit 612 does not comprise a number of available memory segments in the first memory block. Similarly, bit 602 is in state "0" which merely indicates that memory sections in Bitmap 1 604 are available. However, nowhere in

Goldberg is there any teaching that bit 602 indicates that 5 memory sections in Bitmap 1 604 are available. As such, the first state of bit 602 does not comprise a number of available memory segments in the first memory block. In the same way, the first bit (i.e., far left) in Bitmap 1 604 is in state "0" which merely indicates that memory sections in LLB 400 (on far left bottom) are available. However, nowhere in Goldberg is there any teaching that the first bit in Bitmap 1 604 indicates the number of available memory segments in far left bottom LLB 400. As such, the first state of bit 612 does not comprise a number of available memory segments in the first memory block. (*See also*, Goldberg, Figure 5 (bit 502 corresponds with LLB 402, 504 corresponds with 404, etc, – nowhere in Goldberg is there any disclosure that bits 502 and 504 indicate the number of available memory segments in 402 and 404, respectively). Put simply, nowhere in Goldberg is there any disclosure that any of the bits in any of bitmaps 1, 2 and 3 comprises a number of available memory sections/segments in LLB or a lower level bitmap as alleged in the Office Action.

Third, Applicant respectfully submits that the proposed combination of references fails to teach, suggest, or disclose at least, for example, "**wherein the second state of the first logic circuit comprises an offset to available memory**," as set forth in Applicant's independent claim 13.

The November 5, 2009 Office Action alleged that "the pending claims do not require the second state of the first logic circuit to point to an absolute address, but merely to comprise information indicating an offset to available memory." (Office Action mailed November 5, 2009, Page 24, Lines 12-14). Despite noting that "information indicating an offset to available memory" is different than an offset to a starting point for a search for available memory as disclosed by Lehman, the Applicant previously amended independent claim 13 by canceling the noted "information indicating" language to clarify that **the offset is to available memory, not merely a hint or starting point to look for available memory**. As stated in Lehman and acknowledged by the Office Action, Lehman merely discloses "['pointer array 124 permits the data manager to determine immediately if it should look in a given allocation page for a given buddy segment size and **provide a place to start looking for a segment** of a particular size' (Col. 9, lines 53-60)

wherein 'the pointer array 124 **might** point to a buddy segment that is available...but on other occasions **the pointer array might point to a segment that was recently allocated**.... Hence the pointer array actually provides a hint to the location of a free buddy segment. Nevertheless, the pointer for a particular buddy size is guaranteed to be at least **a correct starting point for a search** for that size buddy segment' (Col. 10, lines 1-10) (Figure 7 and related text)]." (Office Action, Point 21, Page 20, Line 20 – Page 21, Line 6 (emphasis added)). Further, the Applicant appreciates the Examiner's recognition that Goldberg "doesn't expressly disclose the second state of the first logic circuit comprise information indicating an offset to available memory." (Office Action, Point 21, Page 20, Lines 17-18).

Despite the Applicant's previous amendment, the current Office Action maintains the rejections because the Office Action alleges that Lehman's pointer might sometimes point to a buddy segment that is available. (Office Action, Point 31, Page 31, Line 14 – Page 31, Line 2). However, the Applicant notes that the Applicant's claim limitations do not recite a second state of a first logic circuit that might sometimes provide an offset to available memory. As such, Lehman's disclosure fails to teach the Applicant's claim limitations. Because (1) Lehman's disclosure of using pointers to provide a place to start looking for a segment fails to remedy the deficiencies of Goldberg in that the combination of references clearly fails to teach "**wherein the second state of the first logic circuit comprises an offset to available memory**," and (2) Goldberg teaches away from using the pointer array structure disclosed by Lehman, a rejection under 35 U.S.C. §103(a) cannot be maintained.

The Applicant respectfully submits that, based upon the above, the proposed combination of Goldberg in view of Lehman fails to teach or suggest by themselves or in combination all of the limitations of Applicant's independent claims 10, 13 and 26, and that the rejections of claims 10, 13 and 26 under 35 U.S.C. §103(a) cannot be maintained. Therefore, Applicant respectfully requests that the rejections of claims 10, 13 and 26 under 35 U.S.C. §103(a), be withdrawn.

Because dependent claims 12, 14-15 and 27 depend, directly or indirectly, from

independent claims 10, 13 or 26, and because claims 10, 13 and 26 are allowable over the proposed combination of references, the Applicant asserts that claims 12, 14-15 and 27 are also allowable over the proposed combination of references and that the rejections of dependent claims 12, 14-15 and 27 are now moot. The Applicant further submits that each of claims 12, 14-15 and 27 is independently allowable. Thus, the Applicant respectfully requests that the rejections of claims 10, 12, 13-15 and 26-27 under 35 U.S.C. §103(a), be withdrawn.

Final Matters

The Office Action makes various statements regarding former claims 1-10, 12-15, 24 and 26-27, 35 U.S.C. § 112, first paragraph, 35 U.S.C. § 103(a), the Goldberg reference, the Lehman reference, the Rozario reference, one of ordinary skill in the art, etc. that are now moot in view of the above-mentioned amendments and/or arguments. Thus, the Applicants will not address all of such statements at the present time. However, the Applicants expressly reserve the right to challenge such statements in the future should the need arise (e.g., if such statements should become relevant by appearing in a rejection of any current or future claim).

Applicant reserves the right to argue additional reasons supporting the allowability of claims 10, 12-15 and 26-27 should the need arise in the future.

CONCLUSION

Applicant respectfully submits that claims 10, 12-15 and 26-27 are in condition for allowance, and requests that the application be passed to issue.

Should anything remain in order to place the present application in condition for allowance, the Examiner is kindly invited to contact the undersigned at the telephone number listed below.

Please charge any required fees not paid herewith or credit any overpayment to the Deposit Account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

Date: August 3, 2010

Respectfully submitted,

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